Curriculum vitae of Francesco Driussi

Francesco Driussi was born in Martignacco (Italy) on November the 27th, 1975.

Contacts: e.mail francesco.driussi@uniud.it; mob. +39 3346671365

Education

2000: Laurea in Ingegneria Gestionale, Università degli Studi di Udine (Italy), 110/110 e lode;
2004: Ph.D. in Electronics, Università degli Studi di Udine (Italy).

Academic Positions and Qualification

2005 – 2018: Research Associate at DIEGM, Università degli Studi di Udine (Italy)
2012: "Abilitazione Scientifica Nazionale" to Associate Professor of Electronics (IINF-01/A Elettronica)
2018 – present: Associate Professor of Electronics at DPIA, Università degli Studi di Udine (Italy)
2024: "Abilitazione Scientifica Nazionale" to Full Professor of Electronics (IINF-01/A Elettronica)

Teaching activities

Courses

2011 – 2018: "Analog Electronics II" (6 CFU), *Ingegneria Elettronica*, Università degli Studi di Udine;
2011 – 2015: "Fundaments of Electronics" (6 CFU), *Ingegneria Gestionale*, Università degli Studi di Udine;
2013/2014: "Analog/digital electronics", *Percorsi Abilitanti Speciali*, Università degli Studi di Udine;
2015 – present: "Fundaments of Analog and Digital Electronics" (12 CFU), *Ingegneria Elettronica*, Università degli Studi di Udine;
2018 – 2023: "Electronic Instrumentation" (3 CFU), *Ingegneria Elettronica LM*, Università degli Studi di Udine;
2023 – present: "RF Circuits and Systems" (6 CFU), *Ingegneria Elettronica LM*, Università degli Studi di Udine.

Thesis supervision

Francesco Driussi has been Advisor or Co-Advisor of more than 25 Thesis for the MS/BS degree in Engineering.

Activities in the Ph.D. programs

2009 – present: member of the "Collegio di Dottorato" for the Ph.D. program in Industrial and Information Engineering of the DPIA/DIEGM, University of Udine, Italy.
2016 – present: he held the course of "Atomistic models and application to Egineering" for the Ph.D. program in Industrial and Information Engineering of the DPIA/DIEGM, University of Udine, Italy.
2020: Committee member for the selection of candidates for the Ph.D. program in Industrial and Information Engineering of the DPIA/DIEGM, University of Udine, Italy.

He is or has been supervisor or co-supervisor of 7 Ph.D. students for the Ph.D. program in Industrial and Information Engineering of the DPIA/DIEGM, University of Udine, Italy.

Boards and responsibility at DPIA, University of Udine, Italy

ERASMUS: Francesco Driussi is responsible for 7 agreements for Student exchanges with European Universities.

2018 – present: member of "Commissione Didattica" for the Electronic Engineering courses
2019: member of "Commissione Schede di Dipartimento"

Invited lectures

2010: “Modeling and simulation of charge trap non volatile memory cells”, European SINANO Summer School, Bertinoro, Italy
2013: “FLASH memory devices for gigascale non-volatile storage”, Ph.D. School of *Gruppo Italiano di Elettronica*, Udine, Italy
2013: “FLASH memory devices for gigascale non-volatile storage”, Royal Institute of Technology (KTH), Stockholm, Sweden
2018: “Fundamentals of Analog and Digital Electronics”, Summer School of Modern Mechatronics, Udine, Italy

Research activities

Research interests

His expertise includes device level characterization and physics-based modeling of transistors and memory cells, with special focus on new devices and materials for advanced CMOS and more-than-Moore application. In particular, he is an expert in the design of experiments and development of characterization techniques for the understanding of physical mechanisms involved in the operation of nano and microelectronic devices. Regarding the modeling activity, Francesco Driussi is an expert in physics-based and statistical models for the simulation of Non-Volatile memories and 2D materials-based devices. Recently, his research activity includes characterization and modeling of x-ray photodiodes and ferroelectric memristors for neuromorphic computing. At the moment, he is also involved in the modeling and characterization of the impact of Dielectric Absorption on the ADC performance.

Research positions

2002 – 2003: Visiting Scientist at Philips Research Leuven inside the IMEC research center (Belgium)
2000 and 2002: Visiting student at ST Microelectronics, design of non-volatile memory cells, Agrate Brianza (Italy)

Experience in European and Italian Competitive Projects

Francesco Driussi is *Responsible/Principal Investigator* for the Udine Research Unit in the following project funded by the Italian MIUR:

- PRIN 2022 – 20227N9LW7 (2023-2025), Fully-digital 3D imager for gamma and hard-X rays

Francesco Driussi is or was also involved as *Scientific Collaborator/Responsible for Deliverables* in the following Competitive Research Projects funded by the EU:

- FIXIT, Horizon Europe, GA: 101135398 (2023-2027)
- ATTOSWITCH, Horizon Europe, GA: 101135571 (2024-2027)
- BeFerroSynaptic, H2020, GA: 871737 (2020-2023);
- E^{2}SWITCH, 7FP – STREP, GA: 619509 (2013-2017);
- GRADE, 7FP – STREP, GA: 317839 (2012-2015);
- STEEPER, 7FP – STREP, GA: 257267 (2010-13);
- MODERN, European ENIAC-JTI, (2009-12);
- NANOSIL, 7FP – Network of Excellence, GA: 21671 (2008-11);
- GRAND, 7FP – STREP, GA: 215752 (2008-11);
- GOSSAMER, 7FP – Integrated Project, GA: 214431 (2008-11);
- PULLNANO, 6FP – Integrated Project, (2006-08);
- SINANO, 6FP – Network of Excellence, IST-506844 (2004-07).

He is or was also involved as *Scientific Collaborator/Responsible for Deliverables* in the following projects funded by the Italian MIUR:

- PRIN 2017 – 2017SRYEJH (2020-23);
- PRIN 2015 – 2015WMZ5C8 (2017-20);
- FIRB 2010 – RBFR10XQ28 (2012-15);
- FIRB 2006 – RBIP06YSJJ (2007-10);
- FIRB 2001 – RBNE012N3X (2003-07).

Francesco Driussi is in the REPRISE expert database of MUR and he served as *Reviewer* for the projects applying to the PRIN 2015 and PRIN 2017 calls.

Research Grants/Funds by industrial partners

Francesco Driussi is or was in charge for the following R&D contracts:

- R&D Agreement nr. 6000014019 “Simulation of Dielectric Absorption impact on ADC converters” (3/2024 – 10/2024), with Infineon Technologies Austria, amount 21000 EUR.
- R&D Agreement nr. 6000014118 “Modeling and characterization of the Dielectric Absorption impact on ADC converters” (11/2024 – 10/2027), with Infineon Technologies Austria, amount 90000 EUR.

Research collaborations

During his research activity, Francesco Driussi has actively collaborated with important *Semiconductor companies* and European Research Laboratories, such as:

- Infineon Technologies, Austria
- NXP (former Philips Semiconductors), the Netherlands
- ST Microelectronics, Italy
- Micron, Italy
- CEA-Leti, France
- IMEC, Belgium
- KTH, Sweden
- NaMLab, Germany
- AMICA-AMO, Germany
- IMM-CNR Lab., Italy
- Elettra, Italy.

His collaborations are also with important *Italian and European Universities*, such as:

- University of Bologna,
- University of Pisa,
- University of Modena and Reggio Emilia
- Polytechnic of Milano,
- Polytechnic of Grenoble (France),
- University of Siegen (Germany),
- University of Aachen (Germany),
- University of Bordeaux.

Editorial boards

2022 – present: *Associate Editor* for "Frontiers in Electronics" (EISSN 2673-5857), editor Frontiers
2023 – present: *Associate Editor* for "Electronics" (EISSN 2079-9292), editor MDPI

2014: co-editor of “Proc. of Int. Conf. on Microelectronic Test Structures (ICMTS) 2014”, ISBN: 978-1-4799-2193-5
2015: co-editor of “Book of Abstracts of Insulating Films on Semiconductor (INFOS) 2015”, ISBN: 978-88-9030-695-2
2015: Guest editor of Microelectronic Engineering (vol. 147, Nov. 2015, ISSN 0167-9317), editor Elsevier
2022: Guest editor of Solid State Electronics (vol. 194, Aug. 2022, ISSN 0038-1101), editor Elsevier
2023: Guest editor of Solid State Electronics (vol. 201, Mar. 2023, ISSN 0038-1101), editor Elsevier

Francesco Driussi serves as *reviewer* for the International Journals: IEEE Transaction on Electron Devices, IEEE Electron Device Letters, IEEE Journal of Electron Device Society, IEEE Transactions on Nanotechnology, Solid State Electronics (Elsevier), Microelectronic Engineering (Elsevier), Microelectronics Reliability (Elsevier), Thin Solid Films (Elsevier), Semiconductor Science and Technology (IOP), Applied Physics Express (IOP), Advanced Electronic Materials (Wiley), The Journal of Physical Chemistry (ACS), ACS Applied Materials & Interfaces (ACS), ACS Nano (ACS), Journal of Physics: Material (IOP), 2D Materials (IOP), Journal of Physics D: Applied Physics (IOP), IEEE Photonics Journal, Materials Science in Semiconductor Processing, Nanomaterials, Superlattices and Microstructures.

Technical and organizing committees of International Conferences

Francesco Driussi is or has been part of the Technical Program Committee for:

2013 – 2014: International Electron Devices Meeting (IEDM), organized by IEEE
2018 – present: International Conference on Microelectronic Test Structures (ICMTS), sponsored by IEEE

He has contributed to the following international conferences as:

2024: *Technical Program Chairman* of 36th Int. Conf. on Microelectronic Test Structures, ICMTS, Edinburgh (UK)
2023: *Session Chairman* of 35th International Conference on Microelectronic Test Structures, ICMTS, Tokyo (JAP)
2022: *Session Chairman* of 8th Joint International EuroSOI-ULIS Conference, Udine (ITA)
2020: *Tutorials Chairman* of 33th International Conference on Microelectronic Test Structures, ICMTS, online
2019: *Session Chairman* of 32th Int. Conference on Microelectronic Test Structures, ICMTS, Kitakyushu (JAP)
2019: *Publication Chairman* of 24th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Udine (ITA)
2018: *Session Chairman* of 31th International Conference on Microelectronic Test Structures, ICMTS, Austin (USA)
2015: *Local Arrangement Chair* of 19th Insulating Films on Semiconductor (INFOS), Udine (ITA)
2014: *Local Arrangement Chair* of 27th Int. Conference on Microelectronic Test Structures, ICMTS, Udine (ITA)
2013: *Local Arrangement Chair* of 45th Annual Meeting of “Gruppo Elettronica” Association, Udine (ITA)
2008: *Local Arrangement Chair* of International Conference on Ultimate Integration on Silicon (ULIS), Udine (ITA)
2001: *Organizing Team member* of 12th Insulating Films on Semiconductor (INFOS), Udine (ITA)

Publications and metrics (as at 14/11/2024)

Below the short report of the peer-reviewed articles in Scientific Journals and Conference Proceedings

Database	Journal articles	Conference papers	Total	Citations	h-index
WOS	65	42	107	1091	18
SCOPUS	66	50	116	1292	20
Google Scholar	n.a.	n.a.	123	1668	22

Index	value	Full professorship reference	Commissioner reference
Articles	37	18	28
Citations last 15 years	1017	462	991
H index last 15 years	18	13	17

Francesco Driussi scientific production has received more than 1300 citations in total. The 16% of his articles are in the top 25% of most cited documents worldwide (font Scopus). The 39% of his papers is in the top 25% journals by CiteScore.

The updated list of Francesco Driussi's publications can be found in the IRIS database.

Scientific articles on peer-reviewed international journals

J1 Lizzit, D.; Pala, M.; Driussi, F.; Esseni, D. Reinterpreting Low Resistance in Sb–MoS2 Ohmic Contacts by Means of Ab Initio Transport Simulations. IEEE TRANSACTIONS ON ELECTRON DEVICES 2024, 71 (5), 3301–3306. https://doi.org/10.1109/ted.2024.3381572.

J2 Lizzit, D.; Khakbaz, P.; Driussi, F.; Pala, M.; Esseni, D. Ohmic Behavior in Metal Contacts to n/p-Type Transition-Metal Dichalcogenides: Schottky versus Tunneling Barrier Trade-Off. ACS APPLIED NANO MATERIALS 2023, 6 (7), 5737–5746. https://doi.org/10.1021/acsanm.3c00166.

J3 Massarotto, M.; Driussi, F.; Affanni, A.; Lancaster, S.; Slesazeck, S.; Mikolajick, T.; Esseni, D. Novel Experimental Methodologies to Reconcile Large- and Small-Signal Responses of Hafnium-Based Ferroelectric Tunnel Junctions. SOLID-STATE ELECTRONICS 2023, 200. https://doi.org/10.1016/j.sse.2022.108569.

J4 Colja, M.; Cautero, M.; Arfelli, F.; Bertolo, M.; Biasiol, G.; Dal Zilio, S.; Driussi, F.; Menk, R. H.; Modesti, S.; Palestri, P.; Pilotto, A.; Cautero, G. Experimental Characterization of Separate Absorption–Multiplication GaAs Staircase Avalanche Photodiodes under Continuous Laser Light Reveals Periodic Oscillations at High Gains. PHOTONICS 2023, 10 (8). https://doi.org/10.3390/photonics10080933.

J5 Colja, M.; Cautero, M.; Menk, R. H.; Palestri, P.; Gianoncelli, A.; Antonelli, M.; Biasiol, G.; Zilio, S. D.; Steinhartova, T.; Nichetti, C.; Arfelli, F.; De Angelis, D.; Driussi, F.; Bonanni, V.; Pilotto, A.; Gariani, G.; Carrato, S.; Cautero, G. Study of Gain, Noise, and Collection Efficiency of GaAs SAM-APDs Single Pixel. JOURNAL OF INSTRUMENTATION 2022, 17 (12). https://doi.org/10.1088/1748-0221/17/12/C12020.

J6 Pilotto, A.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Cautero, G.; Cautero, M.; Colja, M.; Driussi, F.; Esseni, D.; Menk, R. H.; Nichetti, C.; Rosset, F.; Selmi, L.; Steinhartova, T.; Palestri, P. Modeling Approaches for Gain, Noise and Time Response of Avalanche Photodiodes for X-Rays Detection. FRONTIERS IN PHYSICS 2022, 10. https://doi.org/10.3389/fphy.2022.944206.

J7 Massarotto, M.; Driussi, F.; Affanni, A.; Lancaster, S.; Slesazeck, S.; Mikolajick, T.; Esseni, D. Versatile Experimental Setup for FTJ Characterization. SOLID-STATE ELECTRONICS 2022, 194. https://doi.org/10.1016/j.sse.2022.108364.

J8 Khakbaz, P.; Driussi, F.; Giannozzi, P.; Gambi, A.; Lizzit, D.; Esseni, D. Engineering of Metal-MoS2 Contacts to Overcome Fermi Level Pinning. SOLID-STATE ELECTRONICS 2022, 194. https://doi.org/10.1016/j.sse.2022.108378.

J9 Colja, M.; Cautero, M.; Menk, R. H.; Palestri, P.; Gianoncelli, A.; Antonelli, M.; Biasiol, G.; Dal Zilio, S.; Steinhartova, T.; Nichetti, C.; Arfelli, F.; De Angelis, D.; Driussi, F.; Bonanni, V.; Pilotto, A.; Gariani, G.; Carrato, S.; Cautero, G. Synchrotron Radiation Study of Gain, Noise, and Collection Efficiency of GaAs SAM-APDs with Staircase Structure. SENSORS 2022, 22 (12). https://doi.org/10.3390/s22124598.

J10 Segatto, M.; Fontanini, R.; Driussi, F.; Lizzit, D.; Esseni, D. Limitations to Electrical Probing of Spontaneous Polarization in Ferroelectric-Dielectric Heterostructures. IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY 2022, 10, 324–333. https://doi.org/10.1109/JEDS.2022.3164652.

J11 Fontanini, R.; Barbot, J.; Segatto, M.; Lancaster, S.; Duong, Q.; Driussi, F.; Grenouillet, L.; Triozon, L.; Coignus, J.; Mikolajick, T.; Slesazeck, S.; Esseni, D. Interplay between Charge Trapping and Polarization Switching in BEOL-Compatible Bilayer Ferroelectric Tunnel Junctions. IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY 2022, 10, 593–599. https://doi.org/10.1109/JEDS.2022.3171217.

J12 Fontanini, R.; Segatto, M.; Nair, K. S.; Holzer, M.; Driussi, F.; Hausler, I.; Koch, C. T.; Dubourdieu, C.; Deshpande, V.; Esseni, D. Charge-Trapping-Induced Compensation of the Ferroelectric Polarization in FTJs: Optimal Conditions for a Synaptic Device Operation. IEEE TRANSACTIONS ON ELECTRON DEVICES 2022, 69 (7), 3694–3699. https://doi.org/10.1109/TED.2022.3175684.

J13 Lizzit, D.; Khakbaz, P.; Driussi, F.; Pala, M.; Esseni, D. A Study of Metal-MoS2 Contacts by Using an in-House Developed Ab-Initio Transport Simulator. SOLID-STATE ELECTRONICS 2022, 194. https://doi.org/10.1016/j.sse.2022.108365.

J14 Fontanini, R.; Segatto, M.; Massarotto, M.; Specogna, R.; Driussi, F.; Loghi, M.; Esseni, D. Modelling and Design of FTJs as Multi-Level Low Energy Memristors for Neuromorphic Computing. IEEE JOURNAL OF THE ELECTRON DEVICES SOCIETY 2021, 1–1. https://doi.org/10.1109/JEDS.2021.3120200.

J15 Khakbaz, P.; Driussi, F.; Giannozzi, P.; Gambi, A.; Esseni, D. Simulation Study of Fermi Level Depinning in Metal-MoS2 Contacts. SOLID-STATE ELECTRONICS 2021, 184. https://doi.org/10.1016/j.sse.2021.108039.

J16 Driussi, F.; Venica, S.; Gahoi, A.; Kataria, S.; Lemme, M. C.; Palestri, P. Dependability Assessment of Transfer Length Method to Extract the Metal–Graphene Contact Resistance. IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING 2020, 33 (2), 210–215. https://doi.org/10.1109/TSM.2020.2981199.

J17 Nichetti, C.; Steinhartova, T.; Antonelli, M.; Biasiol, G.; Cautero, G.; Angelis, D. D.; Pilotto, A.; Driussi, F.; Palestri, P.; Selmi, L.; Arfelli, F.; Danailov, M.; Menk, R. H. Effects of p Doping on GaAs/AlGaAs SAM-APDs for X-Rays Detection. JOURNAL OF INSTRUMENTATION 2020, 15 (2), C02013-1-C02013-7. https://doi.org/10.1088/1748-0221/15/02/C02013.

J18 Rosset, F.; Pilotto, A.; Selmi, L.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Cautero, G.; De Angelis, D.; Driussi, F.; Menk, R. H.; Nichetti, C.; Steinhartova, T.; Palestri, P. A Model for the Jitter of Avalanche Photodiodes with Separate Absorption and Multiplication Regions. NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH. SECTION A, ACCELERATORS, SPECTROMETERS, DETECTORS AND ASSOCIATED EQUIPMENT 2020, 977. https://doi.org/10.1016/j.nima.2020.164346.

J19 Gahoi, A.; Kataria, S.; Driussi, F.; Venica, S.; Pandey, H.; Esseni, D.; Selmi, L.; Lemme, M. C. Dependable Contact Related Parameter Extraction in Graphene–Metal Junctions. ADVANCED ELECTRONIC MATERIALS 2020, 6 (10), 2000386-1-2000386–2000389. https://doi.org/10.1002/aelm.202000386.

J20 Pilotto, A.; Nichetti, C.; Palestri, P.; Selmi, L.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Cautero, G.; Driussi, F.; Esseni, D.; Menk, R. H.; Steinhartova, T. Optimization of GaAs/AlGaAs Staircase Avalanche Photodiodes Accounting for Both Electron and Hole Impact Ionization. SOLID-STATE ELECTRONICS 2020, 168. https://doi.org/10.1016/j.sse.2019.107728.

J21 Nichetti, C.; Steinhartova, T.; Antonelli, M.; Cautero, G.; Menk, R. H.; Pilotto, A.; Driussi, F.; Palestri, P.; Selmi, L.; Arfelli, F.; Biasiol, G. Gain and Noise in GaAs/AlGaAs Avalanche Photodiodes with Thin Multiplication Regions. JOURNAL OF INSTRUMENTATION 2019, 14 (1), C01003–C01003. https://doi.org/10.1088/1748-0221/14/01/C01003.

J22 Driussi, F.; Venica, S.; Gahoi, A.; Gambi, A.; Giannozzi, P.; Kataria, S.; Lemme, M. C.; Palestri, P.; Esseni, D. Improved Understanding of Metal–Graphene Contacts. MICROELECTRONIC ENGINEERING 2019, 216. https://doi.org/10.1016/j.mee.2019.111035.

J23 Pilotto, A.; Palestri, P.; Selmi, L.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Cautero, G.; Driussi, F.; Menk, R. H.; Nichetti, C.; Steinhartova, T. A New Expression for the Gain-Noise Relation of Single-Carrier Avalanche Photodiodes With Arbitrary Staircase Multiplication Regions. IEEE TRANSACTIONS ON ELECTRON DEVICES 2019, 66 (4), 1810–1814. https://doi.org/10.1109/TED.2019.2900743.

J24 Venica, S.; Driussi, F.; Gahoi, A.; Palestri, P.; Lemme, M. C.; Selmi, L. On the Adequacy of the Transmission Line Model to Describe the Graphene-Metal Contact Resistance. IEEE TRANSACTIONS ON ELECTRON DEVICES 2018, 65 (4), 1589–1596. https://doi.org/10.1109/TED.2018.2802946.

J25 Badami, O.; Lizzit, D.; Driussi, F.; Palestri, P.; Esseni, D. Benchmarking of 3-D MOSFET Architectures: Focus on the Impact of Surface Roughness and Self-Heating. IEEE TRANSACTIONS ON ELECTRON DEVICES 2018, 65 (9), 3646–3653. https://doi.org/10.1109/TED.2018.2857509.

J26 Spiga, S.; Driussi, F.; Congedo, G.; Wiemer, C.; Lamperti, A.; Cianci, E. Sub-1 Nm Equivalent Oxide Thickness Al-HfO2 Trapping Layer with Excellent Thermal Stability and Retention for Nonvolatile Memory. ACS APPLIED NANO MATERIALS 2018, 1 (9), 4633–4641. https://doi.org/10.1021/acsanm.8b00918.

J27 Nichetti, C.; Pilotto, A.; Palestri, P.; Selmi, L.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Cautero, G.; Driussi, F.; Klein, N. Y.; Menk, R. H.; Steinhartova, T. An Improved Nonlocal History-Dependent Model for Gain and Noise in Avalanche Photodiodes Based on Energy Balance Equation. IEEE TRANSACTIONS ON ELECTRON DEVICES 2018, 65 (5), 1823–1829. https://doi.org/10.1109/TED.2018.2817509.

J28 Venica, S.; Driussi, F.; Vaziri, S.; Palestri, P.; Selmi, L. Graphene Base Transistors with Bilayer Tunnel Barriers: Performance Evaluation and Design Guidelines. IEEE TRANSACTIONS ON ELECTRON DEVICES 2017, 64 (2), 593–598. https://doi.org/10.1109/TED.2016.2636447.

J29 Steinhartova, T.; Nichetti, C.; Antonelli, M.; Cautero, G.; Menk, R. H.; Pilotto, A.; Driussi, F.; Palestri, P.; Selmi, L.; Koshmak, K.; Nannarone, S.; Arfelli, F.; Zilio, S. D.; Biasiol, G. Influence of δ P-Doping on the Behaviour of GaAs/AlGaAs SAM-APDs for Synchrotron Radiation. JOURNAL OF INSTRUMENTATION 2017, 12 (Article Number: C11017), 1–7. https://doi.org/10.1088/1748-0221/12/11/C11017.

J30 Ding, L.; Gnani, E.; Gerardin, S.; Bagatin, M.; Driussi, F.; Selmi, L.; Royer, C. L.; Paccagnella, A. Impact of Bias Conditions on Electrical Stress and Ionizing Radiation Effects in Si-Based TFETs. SOLID-STATE ELECTRONICS 2016, 115 (B), 146–151. https://doi.org/10.1016/j.sse.2015.09.003.

J31 Vaziri, S.; Smith, A. D.; Östling, M.; Lupina, G.; Dabrowski, J.; Lippert, G.; Mehr, W.; Driussi, F.; Venica, S.; Di Lecce, V.; Gnudi, A.; König, M.; Ruhl, G.; Belete, M.; Lemme, M. C. Going Ballistic: Graphene Hot Electron Transistors. SOLID STATE COMMUNICATIONS 2015, 224, 64–75. https://doi.org/10.1016/j.ssc.2015.08.012.
J32 Venica, S.; Driussi, F.; Palestri, P.; Selmi, L. Backscattering and Common-Base Current Gain of the Graphene Base Transistor (GBT). MICROELECTRONIC ENGINEERING 2015, 147, 192–195. https://doi.org/10.1016/j.mee.2015.04.089.
J33 Frégonèse, S.; Venica, S.; Driussi, F.; Zimmer, T. Electrical Compact Modeling of Graphene Base Transistors. ELECTRONICS 2015, 4 (4), 969–978. https://doi.org/10.3390/electronics4040969.
J34 Ding, L.; Gnani, E.; Gerardin, S.; Bagatin, M.; Driussi, F.; Palestri, P.; Selmi, L.; Royer, C. L.; Paccagnella, A. Investigation of Hot Carrier Stress and Constant Voltage Stress in High-κ Si-Based TFETs. IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY 2015, 15 (2), 236–241. https://doi.org/10.1109/TDMR.2015.2423095.
J35 Ding, L.; Elena, G.; Simone, G.; Marta, B.; Driussi, F.; Palestri, P.; Selmi, L.; Cyrille Le, R.; Alessandro, P. Total Ionizing Dose Effects in Si-Based Tunnel FETs. IEEE TRANSACTIONS ON NUCLEAR SCIENCE 2014, 61 (6), 2874–2880. https://doi.org/10.1109/TNS.2014.2367548.
J36 Venica, S.; Driussi, F.; Palestri, P.; Esseni, D.; Sam, V.; Selmi, L. Simulation of DC and RF Performance of the Graphene Base Transistor. IEEE TRANSACTIONS ON ELECTRON DEVICES 2014, 61 (7), 2570–2576. https://doi.org/10.1109/TED.2014.2325613.
J37 Driussi, F.; Sabina, S.; Alessio, L.; Gabriele, C.; Gambi, A. Simulation Study of the Trapping Properties of HfO2-Based Charge-Trap Memory Cells. IEEE TRANSACTIONS ON ELECTRON DEVICES 2014, 61 (6), 2056–2063. https://doi.org/10.1109/TED.2014.2316374.
J38 Driussi, F.; Palestri, P.; Selmi, L. Modeling, Simulation and Design of the Vertical Graphene Base Transistor. MICROELECTRONIC ENGINEERING 2013, 109 (9), 338–341. https://doi.org/10.1016/j.mee.2013.03.134.
J39 Spiga, S.; Driussi, F.; Lamperti, A.; Congedo, G.; Salicio, O. Effects of Thermal Treatments on the Trapping Properties of HfO2 Films for Charge Trap Memories. APPLIED PHYSICS EXPRESS 2012, 5 (2), 021102-1-021102–021103. https://doi.org/10.1143/APEX.5.021102.
J40 Toniutti, P.; Palestri, P.; Esseni, D.; Driussi, F.; De Michielis, M.; Selmi, L. On the Origin of the Mobility Reduction in N- and p-Metal-Oxide-Semiconductor Field Effect Transistors with Hafnium-Based/Metal Gate Stacks. JOURNAL OF APPLIED PHYSICS 2012, 112 (3), 034502-1-034502–034512. https://doi.org/10.1063/1.4737781.
J41 Vianello, E.; Driussi, F.; Blaise, P.; Palestri, P.; Esseni, D.; Perniola, L.; Molas, G.; De Salvo, B.; Selmi, L. Explanation of the Charge Trapping Properties of Silicon Nitride Storage Layers for NVMs - Part II: Atomistic and Electrical Modeling. IEEE TRANSACTIONS ON ELECTRON DEVICES 2011, 58 (8), 2490–2499. https://doi.org/10.1109/TED.2011.2156407.
J42 Esseni, D.; Driussi, F. A Quantitative Error Analysis of the Mobility Extraction According to the Matthiessen Rule in Advanced MOS Transistors. IEEE TRANSACTIONS ON ELECTRON DEVICES 2011, 58 (8), 2415–2422. https://doi.org/10.1109/TED.2011.2151863.
J43 Vianello, E.; Driussi, F.; Perniola, L.; Molas, G.; Colonna, J. P.; De Salvo, B.; Selmi, L. Explanation of the Charge-Trapping Properties of Silicon Nitride Storage Layers for NVM Devices Part I: Experimental Evidences From Physical and Electrical Characterizations. IEEE TRANSACTIONS ON ELECTRON DEVICES 2011, 58 (8), 2483–2489. https://doi.org/10.1109/TED.2011.2140116.
J44 Iellina, M.; Palestri, P.; Akil, N.; VAN DUUREN, M.; Driussi, F.; Esseni, D.; Selmi, L. A Simulation Study of the Punch-through Assisted Hot Holes Injection Mechanism for Non-Volatile-Memory Cells. IEEE TRANSACTIONS ON ELECTRON DEVICES 2010, 57 (5), 1055–1062. https://doi.org/10.1109/TED.2010.2043396.
J45 Vianello, E.; Bocquet, M.; Driussi, F.; Perniola, L.; Molas, G.; Selmi, L. Program Efficiency and High Temperature Retention of SiN/High-K Based Memories. MICROELECTRONIC ENGINEERING 2009, 86 (7–9), 1830–1833. https://doi.org/10.1016/j.mee.2009.03.023.
J46 Golubovic, D.; van Duuren, M.; Akil, N.; Arreghini, A.; Driussi, F. Analysis of Nitride Storage Non-Volatile Memories with HfSiO(x) Blocking Dielectric and TiN Metal Gate for Low Power Embedded Applications. MICROELECTRONIC ENGINEERING 2009, 86 (10), 1999–2004. https://doi.org/10.1016/j.mee.2009.01.028.
J47 Driussi, F.; Esseni, D. Simulation Study of Coulomb Mobility in Strained Silicon. IEEE TRANSACTIONS ON ELECTRON DEVICES 2009, 56 (9), 2052–2059. https://doi.org/10.1109/TED.2009.2026394.
J48 Schmidt, M.; Lemme, M.; Gottlob, H.; Driussi, F.; Selmi, L.; Kurz, H. Mobility Extraction in SOI MOSFETs with Sub 1 Nm Body Thickness. SOLID-STATE ELECTRONICS 2009, 53 (12), 1246–1251. https://doi.org/10.1016/j.sse.2009.09.017.

J49 Vianello, E.; Driussi, F.; Arreghini, A.; Palestri, P.; Esseni, D.; Selmi, L.; Akil, N.; van Duuren, M. J.; Golubovic, D. S. Experimental and Simulation Analysis of Program/Retention Transients in Silicon Nitride-Based NVM Cells. IEEE TRANSACTIONS ON ELECTRON DEVICES 2009, 56 (9), 1980–1990. https://doi.org/10.1109/TED.2009.2026113.
J50 Driussi, F.; Esseni, D.; Selmi, L.; Hellström, P. E.; Malm, G.; Hållstedt, J.; Östling, M.; Grasby, T. J.; Leadley, D. R.; Mescot, X. On the Electron Mobility Enhancement in Biaxially Strained Si MOSFETs. SOLID-STATE ELECTRONICS 2008, 52 (4), 498–505. https://doi.org/10.1016/j.sse.2007.10.033.
J51 Arreghini, A.; Akil, N.; Driussi, F.; Esseni, D.; Selmi, L.; van Duuren, M. J. Long Term Charge Retention Dynamics of SONOS Cells. SOLID-STATE ELECTRONICS 2008, 52 (9), 1460–1466. https://doi.org/10.1016/j.sse.2008.04.016.
J52 Arreghini, A.; Driussi, F.; Vianello, E.; Esseni, D.; van Duuren, M. J.; Gobulovic, D. S.; Akil, N.; VAN SCHAIJK, R. Experimental Characterization of the Vertical Position of the Trapped Charge in Si Nitride-Based Nonvolatile Memory Cells. IEEE TRANSACTIONS ON ELECTRON DEVICES 2008, 55 (5), 1211–1219. https://doi.org/10.1109/TED.2008.919713.
J53 Driussi, F.; Selmi, L.; Akil, N.; van Duuren, M. J.; van Schaijk, R. Impact of Device Layout and Annealing Process During the Passivation of Interface States in Presence of Silicon Nitride Layers. IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING 2008, 21 (2), 195–200. https://doi.org/10.1109/TSM.2008.2000280.
J54 Golubović, D. S.; Vianello, E.; Arreghini, A.; Driussi, F.; van Duuren, M. J.; Akil, N.; Selmi, L.; Esseni, D. Programme and Retention Characteristics of SONOS Memory Arrays with Layered Tunnel Barrier. SEMICONDUCTOR SCIENCE AND TECHNOLOGY 2008, 23 (7), 075003–075006. https://doi.org/10.1088/0268-1242/23/7/075003.
J55 Vianello, E.; Driussi, F.; Esseni, D.; Selmi, L.; Widdershoven, F.; van Duuren, M. J. Explanation of SILC Probability Density Distributions with Nonuniform Generation of Traps in the Tunnel Oxide of Flash Memory Arrays. IEEE TRANSACTIONS ON ELECTRON DEVICES 2007, 54 (8), 1953–1962. https://doi.org/10.1109/TED.2007.901262.
J56 Palestri, P.; Barin, N.; Brunel, D.; Busseret, C.; Campera, A.; Childs, P. A.; Driussi, F.; Fiegna, C.; Fiori, G.; Gusmeroli, R.; Iannaccone, G.; Karner, M.; Kosina, H.; Lacaita, A. L.; Langer, E.; Majkusiak, B.; Monzio Compagnoni, C.; Poncet, A.; Sangiorgi, E.; Selmi, L.; Spinelli, A. S.; Walczak, J. Comparison of Modeling Approaches for the Capacitance-Voltage and Current Voltage Characteristics of Advanced Gate Stacks. IEEE TRANSACTIONS ON ELECTRON DEVICES 2007, 54 (1), 106–114. https://doi.org/10.1109/TED.2006.887226.
J57 De Michielis, M.; Esseni, D.; Driussi, F. Analytical Models for the Insight into the Use of Alternative Channel Materials in Ballistic Nano-MOSFETs. IEEE TRANSACTIONS ON ELECTRON DEVICES 2007, 54 (1), 115–123. https://doi.org/10.1109/TED.2006.887519.
J58 Francesco, D.; F., W.; David, E.; Luca, S.; van Duuren, M. Experimental Characterization of Statistically Independent Defects in Gate Dielectrics - Part II: Experimental Results on Flash Memory Arrays. IEEE TRANSACTIONS ON ELECTRON DEVICES 2005, 52 (5), 949–954. https://doi.org/10.1109/TED.2005.846350.
J59 Arreghini, A.; Driussi, F.; Esseni, D.; Selmi, L.; van Duuren, M.; van Schaijk, R. New Charge Pumping Model for the Analysis of the Spatial Trap Distribution in the Nitride Layer of SONOS Devices. MICROELECTRONIC ENGINEERING 2005, 80, 333–336. https://doi.org/10.1016/j.mee.2005.04.087.
J60 Driussi, F.; Widdershoven, F.; Esseni, D.; Selmi, L.; van Duuren, M. Experimental Characterization of Statistically Independent Defects in Gate Dielectrics - Part I: Description and Validation of the Model. IEEE TRANSACTIONS ON ELECTRON DEVICES 2005, 52 (5), 942–948. https://doi.org/10.1109/TED.2005.846349.
J61 Driussi, F.; Iob, R.; Esseni, D.; Selmi, L.; van Schaijk, R.; Widdershoven, F. Investigation of the Energy Distribution of Stress-Induced Oxide Traps by Numerical Analysis of the TAT of HEs. IEEE TRANSACTIONS ON ELECTRON DEVICES 2004, 51 (10), 1570–1576. https://doi.org/10.1109/TED.2004.834899.
J62 Driussi, F.; Esseni, D.; Selmi, L. Performance, Degradation Monitors, and Reliability of the CHISEL Injection Regime. IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY 2004, 4 (3), 327–334. https://doi.org/10.1109/TDMR.2004.837208.
J63 Driussi, F.; Esseni, D.; Selmi, L. On the Electrical Monitor for Device Degradation in the CHISEL Stress Regime. IEEE ELECTRON DEVICE LETTERS 2003, 24 (5), 357–359. https://doi.org/10.1109/LED.2003.812552.
J64 Driussi, F.; Esseni, D.; Selmi, L.; Fausto, P. Damage Generation and Location in N- and p-MOSFETs Biased in the Substrate-Enhanced Gate Current Regime. IEEE TRANSACTIONS ON ELECTRON DEVICES 2002, 49 (5), 787–794. https://doi.org/10.1109/16.998585.
J65 Driussi, F.; Esseni, D.; Selmi, L.; Piazza, F. Hot Hole Gate Current in Surface Channel P-MOSFETs. IEEE ELECTRON DEVICE LETTERS 2001, 22 (1), 29–31. https://doi.org/10.1109/55.892434.

Peer-reviewed contributions in Conference proceedings

C1 Lusardi, N.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Bonanno, G.; Brajnik, G.; Carrato, S.; Cautero, M.; Cautero, G.; Costa, A.; Curcio, D.; Zilio, S. D.; Driussi, F.; Garzetti, F.; Geraci, A.; Harutyunyan, V.; Menk, R.; Palestri, P.; Pilotto, A.; Ronconi, E.; Sbuelz, L.; Sergo, R.; Stebel, L. Time-Resolved 3D Imaging with Capacitively Coupled GaAs SAM-APD and Cross-Delay Lines for Hard X-Ray Photon Detection. In 2024 IEEE Nuclear Science Symposium (NSS), Medical Imaging Conference (MIC) and Room Temperature Semiconductor Detector Conference (RTSD); IEEE, 2024; pp 1–2. https://doi.org/10.1109/nss/mic/rtsd57108.2024.10657794.

C2 Saro, S.; Palestri, P.; Caruso, E.; Toniutti, P.; Calabro, R.; Terokhin, S.; Driussi, F. Compact Expression to Model the Effects of Dielectric Absorption on Analog-to-Digital Converters. In 2024 IEEE 36th International Conference on Microelectronic Test Structures (ICMTS); IEEE, 2024. https://doi.org/10.1109/icmts59902.2024.10520681.

C3 Massarotto, M.; Driussi, F.; Bucovaz, M.; Affanni, A.; Lancaster, S.; Slesazeck, S.; Mikolajick, T.; Esseni, D. Analysis and Compensation of the Series Resistance Effects on the Characteristics of Ferroelectric Capacitors. In 2024 IEEE 36th International Conference on Microelectronic Test Structures (ICMTS); IEEE, 2024. https://doi.org/10.1109/icmts59902.2024.10520684.

C4 Massarotto, M.; Segatto, M.; Driussi, F.; Affanni, A.; Lancaster, S.; Slesazeck, S.; Mikolajick, T.; Esseni, D. Bridging Large-Signal and Small-Signal Responses of Hafnium-Based Ferroelectric Tunnel Junctions. In 2023 35th International Conference on Microelectronic Test Structure (ICMTS); IEEE, 2023; pp 1–6. https://doi.org/10.1109/ICMTS55420.2023.10094178.

C5 Lancaster, S.; Segatto, M.; Silva, C.; Max, B.; Mikolajick, T.; Esseni, D.; Driussi, F.; Slesazeck, S. Reducing the Tunneling Barrier Thickness of Bilayer Ferroelectric Tunnel Junctions with Metallic Electrodes. In 2023 Device Research Conference (DRC); 2023; pp 1–2. https://doi.org/10.1109/DRC58590.2023.10187018.

C6 Esseni, D.; Driussi, F.; Lizzit, D.; Massarotto, M.; Segatto, M. Modelling and Simulations of Ferroelectric Materials and Ferroelectric-Based Nanoelectronic Devices : (Invited Paper). In International Conference on Simulation of Semiconductor Processes and Devices, SISPAD; Institute of Electrical, 2023; pp 9–12. https://doi.org/10.23919/SISPAD57422.2023.10319574.

C7 Segatto, M.; Massarotto, M.; Lancaster, S.; Duong, Q. T.; Affanni, A.; Fontanini, R.; Driussi, F.; Lizzit, D.; Mikolajick, T.; Slesazeck, S.; Esseni, D. Polarization Switching and AC Small-Signal Capacitance in Ferroelectric Tunnel Junctions. In ESSDERC 2022 - IEEE 52nd European Solid-State Device Research Conference (ESSDERC); 2022; pp 340–343. https://doi.org/10.1109/ESSDERC55479.2022.9947185.

C8 Lizzit, D.; Khakbaz, P.; Driussi, F.; Pala, M.; Esseni, D. Ab-Initio Transport Simulations Unveil the Schottky versus Tunneling Barrier Trade-off in Metal-TMD Contacts. In 2022 International Electron Devices Meeting (IEDM); Institute of Electrical, 2022; p 28.2.1-28.2.4. https://doi.org/10.1109/IEDM45625.2022.10019449.

C9 Fontanini, R.; Barbot, J.; Segatto, M.; Lancaster, S.; Duong, Q.; Driussi, F.; Grenouillet, L.; Triozon, F.; Coignus, J.; Mikolajick, T.; Slesazeck, S.; Esseni, D. Polarization Switching and Interface Charges in BEOL Compatible Ferroelectric Tunnel Junctions. In Proceedings of ESSDERC; 2021; pp 255–258. https://doi.org/10.1109/ESSDERC53440.2021.9631812.

C10 Esseni, D.; Fontanini, R.; Lizzit, D.; Massarotto, M.; Driussi, F.; Loghi, M. Ferroelectric Based FETs and Synaptic Devices for Highly Energy Efficient Computational Technologies. In 2021 5th IEEE Electron Devices Technology and Manufacturing Conference, EDTM 2021; Institute of Electrical, 2021; pp 1–3. https://doi.org/10.1109/EDTM50988.2021.9420848.

C11 Fontanini, R.; Massarotto, M.; Specogna, R.; Driussi, F.; Loghi, M.; Esseni, D. Modelling and Design of FTJs as High Reading-Impedance Synaptic Devices. In 2021 5th IEEE Electron Devices Technology and Manufacturing Conference, EDTM 2021; Institute of Electrical: 345 E 47TH ST, NEW YORK, NY 10017 USA, 2021; pp 1–3. https://doi.org/10.1109/EDTM50988.2021.9420863.

C12 Pilotto, A.; Driussi, F.; Esseni, D.; Selmi, L.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Carrato, S.; Cautero, G.; De Angelis, D.; Menk, R. H.; Nichetti, C.; Steinhartova, T.; Palestri, P. Full-Band Monte Carlo Simulations of GaAs p-i-n Avalanche PhotoDiodes: What Are the Limits of Nonlocal Impact Ionization Models? In 2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD); Institute of Electrical, 2020; pp 133–136. https://doi.org/10.23919/SISPAD49475.2020.9241632.

C13 Driussi, F.; Pilotto, A.; De Belli, D.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Cautero, G.; Menk, R. H.; Nichetti, C.; Selmi, L.; Steinhartova, T.; Palestri, P. Experimental and Simulation Analysis of Carrier Lifetimes in GaAs/AlGaAs Avalanche Photo-Diodes. In IEEE International Conference on Microelectronic Test Structures; Institute of Electrical, 2020; Vol. 2020, pp 1–6. https://doi.org/10.1109/ICMTS48187.2020.9107920.

C14 Palestri, P.; Caruso, E.; Badami, O.; Driussi, F.; Esseni, D.; Selmi, L. Semi-Classical Modeling of Nanoscale NMOSFETs with III-V Channel. In 2019 Electron Devices Technology and Manufacturing Conference (EDTM); 2019; pp 234–236. https://doi.org/10.1109/EDTM.2019.8731143.

C15 Nichetti, C.; Steinhartova, T.; Antonelli, M.; Cautero, G.; Menk, R. H.; Pilotto, A.; Driussi, F.; Palestri, P.; Selmi, L.; Arfelli, F.; Biasiol, G. Investigation of the Behaviour of GaAs/AlGaAs SAM-APDs for Synchrotron Radiation. In Proceedings of the 13th International Conference on Synchrotron Radiation Instrumentation – SRI2018; American Institute of Physics Inc., 2019; Vol. 2054. https://doi.org/10.1063/1.5084695.

C16 Khakbaz, P.; Driussi, F.; Gambi, A.; Giannozzi, P.; Venica, S.; Esseni, D.; Gaho, A.; Kataria, S.; Lemme, M. C. DFT Study of Graphene Doping Due to Metal Contacts. In International Conference on Simulation of Semiconductor Processes and Devices (SISPAD). 24th International Conference on Simulation of Semiconductor Processes and Devices, SISPAD 2019; IEEE, 2019; pp 279–282. https://doi.org/10.1109/SISPAD.2019.8870456.

C17 Pilotto, A.; Nichetti, C.; Palestri, P.; Selmi, L.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Cautero, G.; Driussi, F.; Esseni, D.; Menk, R. H.; Steinhartova, T. Optimizing the Number of Steps and the Noise in Staircase APDs with Ternary III - V Semiconductor Alloys. In Proceedings of EUROSOI-ULIS 2019; 2019; pp 1–4. https://doi.org/10.1109/EUROSOI-ULIS45800.2019.9041888.

C18 Pilotto, A.; Palestri, P.; Selmi, L.; Antonelli, M.; Arfelli, F.; Biasiol, G.; Cautero, G.; Driussi, F.; Menk, R. H.; Nichetti, C.; Steinhartova, T. An Improved Random Path Length Algorithm for P-i-n and Staircase Avalanche Photodiodes. In Proceedings of the 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD); IEEE, 2018; pp 26–30. https://doi.org/10.1109/SISPAD.2018.8551751.

C19 Venica, S.; Driussi, F.; Gahoi, A.; Kataria, S.; Palestri, P.; Lenirne, M. C.; Selmi, L. Reliability Analysis of the Metal-Graphene Contact Resistance Extracted by the Transfer Length Method. In Proceedings of the 2018 IEEE INTERNATIONAL CONFERENCE ON MICROELECTRONIC TEST STRUCTURES; 2018; pp 57–62. https://doi.org/10.1109/ICMTS.2018.8383765.

C20 Esseni, D.; Badami, O. M. H.; Driussi, F.; Lizzit, D.; Pala, M.; Palestri, P.; Rollo, T.; Selmi, L.; Venica, S. New Device Concepts, Transistor Architectures and Materials for High Performance and Energy Efficient CMOS Circuits in the Forthcoming Era of 3D Integrated Circuits. In IEEE Electron Devices Technology and Manufacturing Conference, EDTM 2018 - Proceedings; IEEE, 2018; pp 236–238. https://doi.org/10.1109/EDTM.2018.8421501.

C21 Badami, O.; Driussi, F.; Palestri, P.; Selmi, L.; Esseni, D. Performance Comparison for FinFETs, Nanowire and Stacked Nanowires FETs: Focus on the Influence of Surface Roughness and Thermal Effects. In Technical Digest - International Electron Devices Meeting, IEDM; IEEE: Piscataway, 2017; pp 314–317. https://doi.org/10.1109/IEDM.2017.8268382.

C22 Venica, S.; Driussi, F.; Gahoi, A.; Passi, V.; Palestri, P.; Lemme, M. C.; Selmi, L. Detailed Characterization and Critical Discussion of Series Resistance in Graphene-Metal Contacts. In Proceedings of the 2017 IEEE International Conference on Microelectronic Test Structures; 2017; pp 27–31. https://doi.org/10.1109/ICMTS.2017.7954259.

C23 Venica, S.; Driussi, F.; Palestri, P.; Selmi, L. Simulation Study of the Graphene Base Transistor. In Book of Abstracts of 49TH ANNUAL MEETING OF THE ASSOCIAZIONE SOCIETA ITALIANA DI ELETTRONICA; 2017; pp 11–12.

C24 Venica, S.; Zanato, M.; Driussi, F.; Palestri, P.; Selmi, L. Modeling Electrostatic Doping and Series Resistance in Graphene-FETs. In 2016 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD); Institute of Electrical, 2016; pp 357–360. https://doi.org/10.1109/SISPAD.2016.7605220.

C25 Ding, L.; Gerardin, S.; Paccagnella, A.; Gnani, E.; Bagatin, M.; Driussi, F.; Selmi, L.; Le Royer, C. Effects of Electrical Stress and Ionizing Radiation on Si-Based TFETs. In 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS); 2015; pp 137–140. https://doi.org/10.1109/ULIS.2015.7063792.

C26 Palestri, P.; Caruso, E.; Driussi, F.; Esseni, D.; Lizzit, D.; Osgnach, P.; Venica, S.; Selmi, L. State-of-the-Art Semi-Classical Monte Carlo Method for Carrier Transport in Nanoscale Transistors. In Proceedings of 2015 38th International Convention on Information and Communication Technology, Electronics and Microelectronics, MIPRO 2015; 2015; pp 5–12. https://doi.org/10.1109/MIPRO.2015.7160227.

C27 Venica, S.; Driussi, F.; Palestri, P.; Selmi, L. Backscattering and Common-Base Current Gain of the Graphene Base Transistor (GBT). In Book of Abstracts of 19th Conference on “Insulating Films on Semiconductors”; 2015; pp 229–230.

C28 Venica, S.; Driussi, F.; Palestri, P.; Selmi, L. Graphene Base Transistors with Optimized Emitter and Dielectrics. In 2014 37th International Convention on Information and Communication Technology, Electronics and

Microelectronics (MIPRO): proceedings; IEEE: New York, 2014; pp 33–38. https://doi.org/10.1109/MIPRO.2014.6859528.
C29 Driussi, F.; Palestri, P.; Selmi, L. Modelling, Simulation and Design of the Vertical Graphene Base Transistor. In Book of Abstracts of 18th Conference of Insulating Films on Semiconductors; 2013; pp 132–133.
C30 Datta, A.; Driussi, F.; Esseni, D.; Molas, G.; Nowak, E. Experimental Procedure for Accurate Trap Density Study by Low Frequency Charge Pumping Measurements. In Proceedings of IEEE International Conference on Microelectronic Test Structures (ICMTS); 2011; pp 140–144. https://doi.org/10.1109/ICMTS.2011.5976876.
C31 Cristofoli, A.; DALLA COSTA, A.; Boscardin, M.; Cindro, V.; DALLA BETTA, G. F.; Driussi, F.; Giacomini, G.; Giordani, M.; Palestri, P.; Povoli, M.; Ronchin, S.; Vianello, E.; Selmi, L. Simulations and Electrical Characterization of Double-Side Double Type Column 3D Detectors. In Proceedings Nuclear Science Symposium (NSS) 2011; 2011; pp 518–522.
C32 Toniutti, P.; DE MICHIELIS, M.; Palestri, P.; Driussi, F.; Esseni, D.; Selmi, L. Understanding the Mobility Reduction in MOSFETs Featuring High-κ Dielectrics. In Proceeding of the International Conference on Ultimate Integration on Silicon (ULIS); 2010; pp 65–68.
C33 Vianello, E.; Nowak, E.; Mariolle, D.; Chevalier, N.; Perniola, L.; Molas, G.; Colonna, J.; Driussi, F.; Selmi, L. Direct Probing of Trapped Charge Dynamics in SiN by Kelvin Force Microscopy. In Proceedings of the International Conference on Microelectronic Test Structures (ICMTS); 2010; pp 94–97. https://doi.org/10.1109/ICMTS.2010.5466851.
C34 Vianello, E.; Nowak, E.; Perniola, L.; Driussi, F.; Blaise, P.; Molas, G.; DE SALVO, B.; Selmi, L. A Consistent Explanation of the Role of the SiN Composition on the Program/Retention Characteristics of MANOS and NROM like Memories. In Proceeding of the International Memory Workshop (IMW); 2010; pp 106–109. https://doi.org/10.1109/IMW.2010.5488384.
C35 Spiga, S.; Congedo, G.; Russo, U.; Lamperti, A.; Salicio, O.; Driussi, F.; Vianello, E. Experimental and Simulation Study of the Program Efficiency of HfO2 Based Charge Trapping Memories. In Proceeding of the European Solid State Device Research Conference (ESSDERC); 2010; pp 408–411. https://doi.org/10.1109/ESSDERC.2010.5618194.
C36 Schmidt, M.; Lemme, M. C.; Gottlob, H. D. B.; Kurz, H.; Driussi, F.; Selmi, L. Mobility Extraction of UTB N-MOSFETs down to 0.9 Nm SOI Thickness. In Proceeding of the International Conference on Ultimate Integration on Silicon (ULIS); 2009; pp 27–30. https://doi.org/10.1109/ULIS.2009.4897531.
C37 Driussi, F.; Esseni, D. Revised Analysis of Coulomb Scattering Limited Mobility in Biaxially Strained Silicon MOSFETs. In Proceeding of the European Solid State Device Research Conference (ESSDERC); 2009; pp 468–471. https://doi.org/10.1109/ESSDERC.2009.5331465.
C38 Vianello, E.; Perniola, L.; Blaise, P.; Molas, G.; Colonna, J. P.; Driussi, F.; Palestri, P.; Esseni, D.; Selmi, L.; Rochat, N.; Licitra, C.; Lafond, D.; Kies, R.; Reimbold, G.; DE SALVO, B.; Boulanger, F. New Insight on the Charge Trapping Mechanisms of SiN–Based Memory by Atomistic Simulations and Electrical Modeling. In International Electron Devices Meeting (IEDM) Technical Digest; 2009; pp 83–86. https://doi.org/10.1109/IEDM.2009.5424414.
C39 Vianello, E.; Driussi, F.; Palestri, P.; Arreghini, A.; Esseni, D.; Selmi, L.; Akil, N.; van Duuren, M.; Golubović, D. S. Impact of the Charge Transport in the Conduction Band on the Retention of Si-Nitride Based Memories. In Proceedings European Solid-State Device Research Conference (ESSDERC); 2008; pp 107–110. https://doi.org/10.1109/ESSDERC.2008.4681710.
C40 Driussi, F.; Esseni, D.; Selmi, L.; Hellstrom, P. E.; Malm, G.; Hallstedt, J.; Ostling, M.; Grasby, T. J.; Leadley, D. R.; Mescot, X. Experimental and Simulation Study of the Biaxial Strain and Temperature Dependence of the Electron Mobility Enhancement in Si MOSFETs. In Proceeding of the International Conference on Ultimate Integration on Silicon (ULIS); 2007; pp 21–24.
C41 Driussi, F.; Esseni, D.; Selmi, L.; Schmidt, M.; Lemme, M. C.; Kurz, H.; Buca, D.; Mantl, S.; Luysberg, M.; Loo, R.; Nguyen, D.; Reiche, M. Fabrication, Characterization and Modeling of Strained SOI MOSFETs with Very Large Effective Mobility. In Proceeding of the European Solid State Device Research Conference (ESSDERC) 2007; 2007; pp 315–318. https://doi.org/10.1109/ESSDERC.2007.4430941.
C42 Arreghini, A.; Akil, N.; Driussi, F.; Esseni, D.; Selmi, L.; van Duuren, M. J. Characterization and Modeling of Long Term Retention in SONOS Non Volatile Memories. In Proceeding of the European Solid State Device Research Conference (ESSDERC); 2007; pp 406–409. https://doi.org/10.1109/ESSDERC.2007.4430964.
C43 Arreghini, A.; Driussi, F.; Esseni, D.; Selmi, L.; van Duuren, M. J.; van Schaijk, R. Experimental Extraction of Charge Centroid and of Charge Type in the P/E Operation of SONOS Memory Cells. In Proceedings IEDM 2006; 2006; pp 499–502. https://doi.org/10.1109/IEDM.2006.346823.

C44 Driussi, F.; Selmi, L.; Akil, N.; van Duuren, M. J.; van Schaijk, R. On the Passivation of Interface States in SONOS Test Structures: Impact of Device Layout and Annealing Process. In Proceedings of the IEEE International Conference on Microelectronic Test Structures (ICMTS) 2006; 2006; pp 51–55. https://doi.org/10.1109/ICMTS.2006.1614274.

C45 Vianello, E.; Driussi, F.; Esseni, D.; Selmi, L.; van Duuren, M.; Widdershoven, F. Does Multi Trap Assisted Tunneling Explain the Oxide Thickness Dependence of the Statistics of SILC in FLASH Memory Arrays? In Proceedings of the European Solid State Device Research Conference (ESSDERC); 2006; pp 403–406. https://doi.org/10.1109/ESSDER.2006.307723.

C46 De Michielis, M.; Driussi, F.; Esseni, D. Trade-off between Electron Velocity and Density of States in Ballistic Nano-MOSFETs. In Proceedings of the 35th European Solid State Device Research Conference (ESSDERC); 2005; pp 165–168. https://doi.org/10.1109/ESSDER.2005.1546611.

C47 Driussi, F.; Marcuzzi, S.; Palestri, P.; Selmi, L. Gate Current in Stacked Dielectrics for Advanced FLASH EEPROM Cells. In Proceedings of European Solid State Device Research Conference 2005; 2005; pp 317–320.

C48 Driussi, F.; Esseni, D.; Selmi, L.; van Duuren, M. J.; Widdershoven, F. Experimental Evidence and Statistical Modeling of Cooperating Defects in Stressed Oxides. In Proceedings of European Solid State Device Research Conference (ESSDERC), 2004; IEEE, 2004; pp 209–212.

C49 Driussi, F.; Widdershoven, F.; Esseni, D.; van Duuren, M. J. A New Statistical Model to Extract the Stress Induced Oxide Trap Number and the Probability Density Distribution of the Gate Current Produced by a Single Trap. In International Electron Devices Meeting Technical Digest; 2003; pp 161–164.

C50 Driussi, F.; Iob, R.; Esseni, D.; Selmi, L.; van Schaijk, R.; Widdershoven, F. Spectroscopic Analysis of Trap Assisted Tunneling on This Oxides by Means of Substrate Hot Electron Injection Experiments. In Proceedings of International Electron Devices Meeting (IEDM), 2002; IEEE, 2002; pp 159–162. https://doi.org/10.1109/IEDM.2002.1175803.

C51 Driussi, F.; Esseni, D.; Selmi, L.; Piazza, F.; Sangiorgi, E. Substrate Enhanced Gate Currents in CMOS Devices. In Proceedings of Advances in Silicon Technology and Devices, 2000; 2000.

C52 Driussi, F.; Esseni, D.; Piazza, F.; Selmi, L. Hot Carrier Degradation and Damage Profiling of Cmos Devices with Biased Substrates. In Proceedings of MEDEA/RESPONSE Workshop; 2000.

C53 Driussi, F.; Esseni, D.; Selmi, L.; Piazza, F. Observation of a New Hole Gate Current Component in P+-Poly Gate p-Channel Mosfet's. In Proceedings of European Solid State Device Research (ESSDERC), 2000; 2000; Vol. 30, pp 136–139.

C54 Driussi, F.; Esseni, D.; Selmi, L.; Piazza, F. Substrate Enhanced Degradation of Cmos Devices. In International Electron Devices Meeting Technical Digest; 2000; pp 323–326.

Technical Notes

T1 F. Driussi, M. van Duuren, R. van Schaijk, "Nitride Layer Influence on the Hydrogen Anneal of Interface Dangling Bonds", Philips Research Leuven Technical Note PR-TN-2003/00863, 2003.

Editorial articles

E1 Driussi F., " WELCOME LETTER FROM TECHNICAL CHAIR," *2024 IEEE 36th International Conference on Microelectronic Test Structures (ICMTS)*, Edinburgh, United Kingdom, 2024, pp. I-X, doi: 10.1109/ICMTS59902.2024.10520679.

E2 Francesco Driussi, David Esseni, Daniel Lizzit, Pierpaolo Palestri, "Editorial: Selected papers from the 8th Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS 2022)," Solid-State Electronics, Volume 201, 2023, 108603, ISSN 0038-1101, https://doi.org/10.1016/j.sse.2023.108603.

E3 Francesco Driussi, David Esseni, Daniel Lizzit, Pierpaolo Palestri, "Editorial: Letters from the 8th Joint International EUROSOI workshop and International Conference on Ultimate Integration on Silicon," Solid-State Electronics, Volume 194, 2022, 108354, ISSN 0038-1101, https://doi.org/10.1016/j.sse.2022.108354.

E4 Esseni, D., Palestri P., Rideau D, Driussi F., "SISPAD 2019 Welcome Page," *2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Udine, Italy, 2019, pp. ii-iv, doi: 10.1109/SISPAD.2019.8870376.

E5 Luca Selmi, Johan Klootwijk, Gaudenzio Meneghesso, Alain Toffoli, Francesco Driussi, "Welcome letter," *2014 International Conference on Microelectronic Test Structures (ICMTS)*, Udine, Italy, 2014, pp. i-xii, doi: 10.1109/ICMTS.2014.6841457.

E6 D. Esseni. P. Palestri, L. Selmi, F. Driussi, " Foreword," *2008 9th International Conference on Ultimate Integration of Silicon*, Udine, Italy, 2008, pp. 1-5, doi: 10.1109/ULIS.2008.4527125.